



Name : RAJANI BISHT

Designation : Associate Prof.

Department : Electronics Engg.

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FAX Number :

**Area of Interest**

Major Area: VLSI DESIGN, TFT CIRCUITS, RF CIRCUITS

Minor Area: Microprocessors

### **Personal Profile**

Date of Birth : 03.03.63

Marital Status : Married

Residence : D-48, HBTI WEST CAMPUS, KANPUR

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### Academic Qualifications

Sl. No.	Degree	Year	Institute/ College	University
<b>1.</b>	<b>BE</b>	<b>1984</b>	<b>GEC JABALPUR</b>	<b>Rani Durgawati University Jabalpur</b>
<b>2.</b>	<b>ME</b>	<b>2000</b>	<b>University Of Roorkee, Roorkee</b>	<b>University of Roorkee, Rookee</b>
<b>3.</b>	<b>PHD</b>	<b>Pursuing under QIP</b>	<b>IIT Kanpur</b>	<b>IIT Kanpur</b>

M.Tech. Dissertation: “VLSI interconnect delay minimization using CMOS inverters”

Doctoral Dissertation: “Transceivers for IoT” Pursuing

## Experience Record

Academic:

Sl. No.	Designation	Organization	Duration
1.	Associate Prof.	H.B.T.I. KANPUR	2003 onwards
2	Assistant Prof.	H.B.T.I. KANPUR	1998 to 2003
3	Sr. Lecturer	H B T I KANPUR	18 Oct 1993 to 1998
4	Lecturer	Govt. Engg. College Bhopal	Nov 1990 to 1991
5	Lecturer	Govt Womens Polytechnic Bhopal	July 1987 to 1990 Nov
	Lecturer		Oct 1984 to July 1987
		Govt Polytechnic Durg	

Scientific:

Sl. No.	Designation	Organization	Duration
1	Senior Project Associate	I.I.T. KANPUR	August 1991 to 1992

## **Teaching Records**

### **Courses Taught at PG Level:**

- VLSI SYSTEM DESIGN
- ADVANCED MICROPROCESSORS
- SOLID STATE SEMICONDUCTOR DEVICES
- ADVANCED SEMICONDUCTOR DEVICES

### **Courses Taught at UG Level:**

- VLSI TECHNOLOGY
- VLSI DESIGN
- DIGITAL INTEGRATED CIRCUITS
- ELECTRONICS CIRCUITS & DEVICES
- INTEGRATED CIRCUITED & DEVICES
- MICROELECTRONICS
- ANTEENA & WAVE PROPAGATION
- INDUSTRIAL INSTRUMENTATION
- COMPUTER AIDED DESIGN OF ELECTRONIC CIRCUITS
- COMMUNICATION SYSTEM PRACTICE
- PC HARDWARE
- ADVANCED SEMICONDUCTOR DEVICES
- DIGITAL SYSTEM DESIGN USING VHDL

### **Invited lectures at Other Organizations**

- “VLSI Design & Testing” at Institution of Engineers, Kanpur Chapter on Feb 15<sup>th</sup>, 2004.
- MPEC Kanpur “Overview on VLSI Design”
- AITH Kanpur “ Overview on VLSI Design”

### Administrative Experience

#### Administrative Work:

- 1988-1990 2nd LT. NCC OFFICER GOVT. WOMEN'S POLYTECHNIC BHOPAL
- 1989-1990 WARDEN GOVT. WOMEN'S POLYTECHNIC BHOPAL
- 2005 WARDEN NGH HBTI KANPUR
- Warden GH-IV HBTI Kanpur
- Head Electronics (two terms) HBTI Kanpur
- Warden Gangotri Hostel HBTU Kanpur
- Associate Dean Academic HBTU Kanpur

#### Professional Committee Work:

- 2001, Member, Syllabi making committee, curriculum development of UPTU syllabus of Electronic & Communication, HBTI KANPUR
- 2004, Member, Syllabi making committee, curriculum Revision of UPTU syllabus of Electronic & Communication, HBTI KANPUR
- 2004, Member, Syllabi making committee, curriculum development of Polytechnic syllabus of Electronic & Communication, IRDT, KANPUR
- Member BOS, HBTI Kanpur
- Member BOS, HBTU Kanpur

### Membership of Professional Bodies

Associate Member/Institution of Electronics & Telecommunication Engineers/M138582  
Student Member IEEE/ Membership no. 94904765

#### Research Guidance Guided many U G projects and M. Tech Theses

S. No.	Year	Title of M tech Thesis	Name of Student
1.	2004	Single Precision 32 Bit Pipeline Floating Point Addition & Subtraction in VHDL	Ms. Richa (740/02)
2.	2004	Automatic Test Pattern Generator for Sequential Circuits	Amit Kumar (733/02)
3.	2005	Analog Technique for MOS and TFT Circuits	Sunil Kumar Yadav (720/03)
4.	2005	Process Automation System for Differential Pressure Control of Propellant Tanks in Liquid Rocket Stages	Man Mohan Vaishya (721/03)
5.	2006	Analysis of Tradeoff in CMOS Differential Amplifier	Ajay Bharti (745/04)
6.	2007	Design of I/O Buffer (Slew Rate Controlled) in 65nm CMOS Process	Manoj Kumar Tiwari (721/05)
7.	2007	Analysis of Impact of Kink effect on poly-silicon TFT Analog Circuit & its reduction	Manish Agarwal (702/05)
8.	2010	Analysis and Characterization of Gate Diffusion Input	Arun Prakash Singh (709/07)
9.	2010	Design and Implementation of Fast Adders Using VHDL	Nishi Chandra (729/08)

		and FPGA	
10.	2011	Design of 16 -bit Microprocessor using VHDL	Abhai Shankar Chaurasia (734/09)
11.	2011	Design of Adder using Quaternary Signed Digit Number System	Vishal Pandey (732/09)
12.	2012	Characterization of Low Power MOS SRAM Cells	Ankit Khandelwal (707/10)
13.	2012	Threshold Voltage Compensation for Analog circuit design using TFT	Geeta Awasthi (710/10)
14.	2013	Design of MOS current mode Logic Adder	Koshal Kishor Gupta (707/11)
15.	2013	Low Power CMOS full adder design	Pankaj Verma (709/11)
16.	2014	Design of 8-bit RISC Microprocessor using VHDL	Atul Kumar (723/12)
17.	2014	Floating Point Multiplier Design based on Vedic Multiplication Technique using VHDL	Pankaj Singh (726/12)
18.	2014	Performance Analysis of conventional & Double Gate (DG) MOSFET	Rajesh Kumar (729/12)
19.	2015	Leakage Power Reduction Techniques for CMOS Circuits	Kuldeep Singh (741/13)

### Sponsored Projects

Title	Funding Agency	Amount	Duration
“VLSI Design”,	AICTE,	Rs10.0Lacks,	Three Years

### Publications

Sr. No.	Authors	Title of Paper	Name of Organizer (Institution)	Name of University	Conference Date and Year
1	Rajani Bisht, S. Qureshi	“Design of Low-Power Reconfigurable Low-Noise Amplifier with Enhanced Linearity” (Accepted)	TENCON 2019	Kochi, Kerala	17-20 Oct. 2019
2	Rajani Bisht, B. Mazhari	“Impact of Kink Effect on Performance of Poly-Silicon based TFT Differential Amplifiers”	Asian Symposium on Information Display (ASID)	IIT Kanpur	06 in New Delhi during Oct 8 to Oct 12, 06.
3	Rajani Bisht, S Sarkar, R P Agarwal	“VLSI interconnect delay minimization using CMOS inverters”	IIT, Roorkee	IIT, Roorkee	Proceedings of All India Seminar on Recent Trends in VLSI, 29 <sup>th</sup> -30 <sup>th</sup> September 2001