Name : RAJANI BISHT

Designation : Associate Prof.

Department : Electronics Engg.

Tel. Office : 2534001-05-211
FAX Number :

Area of Interest

Major Area: VLSI DESIGN, TFT CIRCUITS

Minor Area: Microprocessors

Personal Profile

Date of Birth	:	03.03.63
Marital Status	:	Married
Residence	:	D-48, HBTI WEST CAMPUS, KANPUR
Contact Number	:	
Tel. Res.		9415404981
Mobile	:	
E-Mail	:	rajanibisht@rediffmail.com

Academic Qualifications

Sl. No.	Degree	Year	Institute/ College	University
1.	**BE**	**1984**	**GEC JABALPUR**	**Rani Durgawati University Jabalpur**
2.	**ME**	**2000**	**University Of Roorkee, Roorkee**	**University of Roorkee, Rookee**
3.	**PHD**	**Perusing under QIP**	**IIT Kanpur**	**IIT Kanpur**

M.Tech. Dissertation: "VLSI interconnect delay minimization using CMOS inverters"

Doctoral Dissertation: Perusing

Experience Record

Academic:

Sl. No.	Designation	Organization	Duration
1.	Associate Prof.	H.B.T.I. KANPUR	2003 onwards
2	Assistant Prof.	H.B.T.I. KANPUR	1998 10 2003
3	Sr. Lecturer	H B T I KANPUR	18 Oct 1993 to 1998
4	Lecturer Lecturer	Govt. Engg. College Bhopal	Nov 1990 to 1991 July 1987 to 1990 Nov
5	Lecturer Lecturer	Govt Womens Polytechnic Bhopal Govt Polytechnic Durg	Oct 1984 to July 1987

Scientific:

Sl. No.	Designation	Organization	Duration
1	Senior Project Associate	I.I.T. KANPUR	August 1991 to 1992

Teaching Records

Courses Taught at PG Level:

- VLSI SYSTEM DESIGN
- ADVANCED MICROPROCESSORS
- SOLID STATE SEMICONDUCTER DEVICES
- Advanced Semiconductor Devices

Courses Taught at UG Level:

- VLSI TECHNOLOGY
- VLSI DESIGN
- DIGITAL INTEGRATED CIRCUITS
- ELECTRONICS CIRCUITS & DEVICES
- INTEGRATED CIRCUITED &DEVICES
- MICROELECTRONICS
- ANTEENA &WAVE PROPAGATION
- INDUSTRIAL INSTRUMENTATION
- COMPUTER AIDED DESIGN OF ELECTRONIC CIRCUITS
- COMMUNICTION SYSTEM PRACTICE
- PC HARDWARE
- Advanced Semiconductor Devices
- Digital System Design using VHDL

Invited lectures at Other Organizations

- "VLSI Design & Testing" at Institution of Engineers, Kanpur Chapter on Feb 15th , 04.
- MPEC Kanpur " Overview on VLSI Design"
- AITH Kanpur " Overview on VLSI Design"

Administrative Experience

Administrative Work:

- 1988-1990 2nd LT. NCC OFFICER GOVT. WOMEN'S POLYTECHNIC **B**HOPAL
- 1989-1990 WARDEN GOVT. WOMEN'S POLYTECHNIC BHOPAL
- 2005 WARDEN NGH HBTI KANPUR
- Warden GH-IV HBTI Kanpur
- Head Electronics(two terms) HBTI Kanpur

Professional Committee Work:

- 2001,Member,Syllabi making committee, curriculum development of UPTU syllabus of Electronic & Communication, HBTI KANPUR
- 2004, Member, Syllabi making committee, curriculum Revision of UPTU syllabus of Electronic & Communication, HBTI KANPUR
- 2004, Member, Syllabi making committee, curriculum development of Polytechnic syllabus of Electronic & Communication, IRDT, KANPUR

Membership of Professional Bodies

Associate Member/Institution of Electronics & Telecommunication Engineers/M138582

Research Guidance Guided many U G projects and M.Tech Theses

S. No.	Year	Title of M tech Thesis	Name of Student
1.	2004	Single Precision 32 Bit Pipeline Floating Point Addition & Subtraction in VHDL	Ms. Richa (740/02)
2.	2004	Automatic Test Pattern Generator for Sequential Circuits	Amit Kumar (733/02)
3.	2005	Analog Technique for MOS and TFT Circuits	Sunil Kumar Yadav (720/03)
4.	2005	Process Automation System for Differential Pressure Control of Propellant Tanks in Liquid Rocket Stages	Man Mohan Vaishya (721/03)
5.	2006	Analysis of Tradeoff in CMOS Differential Amplifier	Ajay Bharti (745/04)
6.	2007	Design of I/O Buffer (Slew Rate Controlled) in 65nm CMOS Process	Manoj Kumar Tiwari (721/05)
7.	2007	Analysis of Impact of Kink effect on poly-silicon TFT Analog Circuit & its reduction	Manish Agarwal (702/05)
8.	2010	Analysis and Characterization of Gate Diffusion Input	Arun Prakash Singh (709/07)
9.	2010	Design and Implementation of Fast Adders Using VHDL	Nishi Chandra (729/08)

		and FPGA	
10.	2011	Design of 16 -bit Microprocessor using VHDL	Abhai Shankar Chaurasia (734/09)
11.	2011	Design of Adder using Quaternary Signed Digit Number System	Vishal Pandey (732/09)
12.	2012	Characterization of Low Power MOS SRAM Cells	Ankit Khandelwal (707/10)
13.	2012	Threshold Voltage Compensation for Analog circuit design using TFT	Geeta Awasthi (710/10)
14.	2013	Design of MOS current mode Logic Adder	Koshal Kishor Gupta (707/11)
15.	2013	Low Power CMOS full adder design	Pankaj Verma (709/11)
16.	2014	Design of 8-bit RISC Microprocessor using VHDL	Atul Kumar (723/12)
17.	2014	Floating Point Multiplier Design based on Vedic Multiplication Technique using VHDL	Pankaj Singh (726/12)
18.	2014	Performance Analysis of conventional &Double Gate (DG) MOSFET	Rajesh Kumar (729/12)
19.	2015	Leakage Power Reduction Techniques for CMOS Circuits	Kuldeep Singh (741/13)

Sponsored Projects

Title	Funding Agency	Amount	Duration
"VLSI Design",	AICTE,	Rs10.0Lacks,	Three Years

Publications

Sr. No.	Authors	Title of Paper	Name of Organizer (Institution)	Name of University	Conference Date and Year
1	Rajani Bisht, B. Mazhari	"Impact of Kink Effect on Performance of Poly-Silicon based TFT Differential Amplifiers"	Asian Symposium on Information Display (ASID)	IIT Kanpur	06 in New Delhi during Oct 8 to Oct 12, 06.
2	Rajani Bisht, S Sarkar, R P Agarwal	"VLSI interconnect delay minimization using CMOS inverters"	IIT, Roorkee	IIT, Roorkee	1. Proceedings of All India Seminar on Recent Trends in VLSI, (held on 29^{th}-30^{th} September 2001 at.